WHAT IS CLAIMED IS:

1. A driving circuit for a switch-bridge of a DC-DC converter, said switch-bridge comprising a main switch connected in series with an active switch operating in complementary to said main switch, comprising:

an input terminal receiving an input of a PWM signal;

a first output terminal connected to said main switch for outputting a low-side driving signal;

a second output terminal connected to said active switch for outputting a high-side driving signal;

a first branch having a voltage level shifting capacitor and a first buffer connected in series between said input terminal and said second output terminal; and

a second branch having a delay circuit and a second buffer connected in series between said input terminal and said first output terminal;

wherein when said input of said PWM signal drops from a high level to a low level, said input of PWM signal is transmitted to said second buffer through said delay circuit for turning off said main switch and then triggering said first buffer to turn on said active switch, and when said input of PWM signal turns from said low level to said high level, said voltage level shifting capacitor transmits said input of PWM signal to said first buffer for turning off said active switch and then triggering said second buffer to turn on said main switch with a short time delay.

2. The driving circuit according to claim 1, wherein said DC-DC converter is one selected from a group consisting of an active clamp forward converter, an active clamp flyback converter, an active clamp forward-flyback converter, a boost converter, and a boost half bridge converter.

3. The driving circuit according to claim 1, wherein said delay circuit is a leading edge delay circuit and comprising:

a switch having an emitter terminal connected to said input terminal, a collector terminal connected to an output of said delay circuit, and a base terminal connected to a voltage source through a first resistor and connected to the ground through a second resistor;

a capacitor coupled between said base terminal and said emitter terminal of said switch; and

a diode having an anode terminal connected to said collector terminal and a cathode terminal connected to said emitter terminal of said switch.

4. The driving circuit according to claim 3, wherein said switch is a PNP transistor.

5. The driving circuit according to claim 1, wherein said second buffer comprises:

a NPN transistor; and

a PNP transistor, wherein both emitter terminals of said NPN transistor and said PNP transistor are connected to said first output terminal, and both base terminals of said NPN transistor and said PNP transistor are connected to an output terminal of said delay circuit.

6. The driving circuit according to claim 1, wherein said first buffer comprises:

a terminal connected to a source terminal of said active switch;

a first diode and a second diode connected in series with a capacitor coupled between a voltage source and said terminal, which forms a boost trap circuit;

a first transistor having a collector terminal connected to a terminal of said capacitor, a base terminal connected to said collector terminal thereof through a

resistor, and an emitter terminal connected to a gate terminal of said active switch;

a second transistor having a base terminal connected to said voltage level shifting capacitor through a current limited resistor, a collector terminal connected to said base terminal of said first transistor, and an emitter terminal connected to said terminal; and

a third diode and a fourth diode inversely arranged between said base terminal and said emitter terminal of said first transistor and said second transistor respectively.

7. The driving circuit according to claim 6, wherein said first transistor and second transistors are both NPN transistors.

8. The driving circuit according to claim 1, wherein said first buffer comprises:

a first terminal connected to a source terminal of said active switch;

a first diode and a second diode connected in series with a first capacitor coupled between a voltage source and said first terminal, which forms a boost trap circuit;

a first transistor having an emitter terminal connected to a terminal of said capacitor, a base terminal connected to said emitter terminal thereof through a third diode, and a collector terminal connected to a gate terminal of said active switch;

a second terminal connected to a drain terminal of said active switch;

a fourth diode and a fifth diode in series arranged between a cathode terminal of said first diode and said second terminal;

a second capacitor having a terminal connected to said base terminal of said first transistor, and the other terminal connected to a cathode terminal of said fourth diode;

a second transistor having a base terminal connected to said voltage level shifting capacitor through a current limited resistor, a collector terminal connected to said gate terminal of said active switch, and an emitter terminal connected to said first terminal; and

a sixth diode arranged between said base terminal and said emitter terminal of second transistor.

9. The driving circuit according to claim 8, wherein said first transistor is a PNP transistor and said second transistor is a NPN transistor.

10. An active clamp DC/DC converter, comprising:

a transformer;

a main switch connected in series with a primary winding of said transformer;

an active clamp branch having an active switch which operates in complementary to said main switch and a clamping capacitor which is connected in parallel with said primary winding of said transformer; and

a driving circuit comprising:

an input terminal receiving an input of a PWM signal;

a first output terminal connected to said main switch for outputting a low-side driving signal;

a second output terminal connected to said active switch for outputting a high-side driving signal;

a first branch having a voltage level shifting capacitor and a first buffer in series between said input terminal and said second output terminal; and

a second branch having a delay circuit and a second buffer in series between said input terminal and said first output terminal;

wherein when said input of said PWM signal drops from a high level to a low level, said input of PWM signal is transmitted to said second buffer through said delay circuit for turning off said main switch and then triggering said first buffer to turn on said active switch, and when said input of PWM signal turns from said low level to said high level, said voltage level shifting capacitor transmits said input of PWM signal to said first buffer for turning off said active switch and then triggering said second buffer to turn on said main switch with a short time delay.

11. The active clamp DC/DC converter according to claim 10, wherein said delay circuit which is a leading edge delay circuit and comprising:

a switch having an emitter terminal connected to said input terminal, a collector terminal connected to an output of said delay circuit, and a base terminal connected to a voltage source through a first resistor and connected to the ground through a second resistor;

a capacitor coupled between said base terminal and said emitter terminal of said switch; and

a diode having an anode terminal connected to said collector terminal and a cathode terminal connected to said emitter terminal of said switch.

12. The active clamp DC/DC converter according to claim 11, wherein said switch is a PNP transistor.

13. The active clamp DC/DC converter according to claim 10, wherein said second buffer comprises:

a NPN transistor; and

a PNP transistor, wherein both emitter terminals of said NPN transistor and said PNP transistor are connected to said first output terminal, and both base

terminals of said NPN transistor and said PNP transistor are connected to an output terminal of said delay circuit.

14. The active clamp DC/DC converter according to claim 10, wherein said first buffer comprises:

a terminal connected to a source terminal of said active switch;

a first diode and a second diode connected in series with a capacitor coupled between a voltage source and said terminal, which forms a boost trap circuit;

a first transistor having a collector terminal connected to a terminal of said capacitor, a base terminal connected to said collector terminal thereof through a resistor, and an emitter terminal connected to a gate terminal of said active switch;

a second transistor having a base terminal connected to said voltage level shifting capacitor through a current limited resistor, a collector terminal connected to said base terminal of said first transistor, and an emitter terminal connected to said terminal; and

a third diode and a fourth diode inversely arranged between said base terminal and said emitter terminal of said first transistor and said second transistor respectively.

15. The active clamp DC/DC converter according to claim 14, wherein said first transistor and second transistors are both NPN transistors.

16. The active clamp DC/DC converter according to claim 10, wherein said first buffer comprises:

a first terminal connected to a source terminal of said active switch;

a first diode and a second diode connected in series with a first capacitor coupled between a voltage source and said first terminal, which forms a boost trap circuit;

a first transistor having an emitter terminal connected to a terminal of said capacitor, a base terminal connected to said emitter terminal thereof through a third diode, and a collector terminal connected to a gate terminal of said active switch;

a second terminal connected to a drain terminal of said active switch;

a fourth diode and a fifth diode in series arranged between a cathode terminal of said first diode and said second terminal;

a second capacitor having a terminal connected to said base terminal of said first transistor, and the other terminal connected to a cathode terminal of said fourth diode;

a second transistor having a base terminal connected to said voltage level shifting capacitor through a current limited resistor, a collector terminal connected to said gate terminal of said active switch, and an emitter terminal connected to said first terminal; and

a sixth diode arranged between said base terminal and said emitter terminal of second transistor.

17. The driving circuit according to claim 16, wherein said first transistor is a PNP transistor and said second transistor is a NPN transistor.

18. A voltage level shifting method for a driving circuit of a switch-bridge in a DC-DC converter, wherein said switch-bridge comprises a main switch connected in series with an active switch operating in complementary to said main switch, said driving circuit comprises a first branch having a voltage level shifting capacitor and a first buffer connected in series between an input

terminal and a second output terminal, and a second branch having a delay circuit and a second buffer connected in series between said input terminal and a first output terminal, comprising the steps of:

receiving an input of PWM signal;

transmitting said input of PWM signal to said second buffer through said delay circuit to turn off said main switch and then to trigger said first buffer to turn on said active switch if said input of said PWM signal drops from a relatively higher level to a relatively lower level; and

transmitting said input of PWM signal to said first buffer at said voltage level shifting capacitor to turn off said active switch and then to trigger said second buffer to turn on said main switch with a short time delay if said input of said PWM signal turns from a relatively lower level to a relatively higher level.

19. The method according to claim 18, wherein said voltage level shifting method further comprises the steps of:

receiving said input of PWM signal at said input terminal;

outputting a low-side driving signal at said first output terminal; and

outputting a high-side driving signal at said second output terminal.

20. The method according to claim 18, wherein said DC-DC converter is one selected from a group consisting of an active clamp forward converter, an active clamp flyback converter, an active clamp forward-flyback converter, a boost converter, and a boost half bridge converter.